In the Claims:

This listing of claims replaces all prior versions.

1. (*Previously presented*) Method for manufacturing on a substrate a semiconductor device with a floating-gate and a control-gate, comprising the steps of:

first forming isolation zones in the substrate,

thereafter forming a floating gate on the substrate between two of the isolation zones,

thereafter extending the floating gate using conductive spacers, and

thereafter forming a control gate over the floating gate and the conductive spacers.

2. (*Previously presented*) Method according to claim 1, wherein the step of forming the floating gate comprises:

providing the floating gate on the substrate, the floating gate having two opposite walls located above the isolation zones, and

forming recesses in the isolation zones under the opposite walls of the floating gate.

3. (*Previously presented*) Method according to claim 2, wherein the step of providing the floating gate, comprises:

depositing a floating gate layer, and

forming slits in the floating gate layer, thus forming the opposite walls of the floating gate.

4. (*Previously presented*) Method according to claim 2, wherein the step of extending the floating gate comprises depositing a conductive layer on the opposite walls of the floating gate and on walls of the recesses in the isolation zones.

5. (*Previously presented*) Method according to claim 4, wherein the step of depositing a conductive layer on the opposite walls of the floating gate and on the walls of the recesses in the isolation zones comprises:

depositing a conductive layer over the floating gate and in the recesses in the isolation zones, and

etching the conductive layer.

6. (*Original*) Method according to claim 1, further comprising a step of forming a dielectric layer on the floating gate and on the conductive spacers before forming the control gate.

7. (*Original*) Method according to claim 1, wherein the isolation zones are shallow trench isolation (STI) zones.

8. (*Original*) Method according to claim 1, wherein the isolation zones are LOCOS regions.

9. (*Original*) Method according to claim 2, wherein a recess in an isolation zone is formed by etching.

10. (*Previously presented*) Method according to claim 1, further comprising a step of providing a tunnel oxide between the semiconductor substrate and the floating gate.

11. (*Previously presented*) Method according to claim 1, wherein the step of forming the control gate comprises:

depositing a control gate layer, and

patterning the control gate layer to form the control gate.

12. (*Original*) Method according to claim 1, wherein the conductive spacers are polysilicon spacers.

Claims 13-18 (*Cancelled*)